BeastLink Overview

BeastLink is a set of ready made components that allow fast, fail safe transfer between AXI-4 peripherals inside a Xilinx 7 Series FPGA and a PC. Transfer is handled with USB 3.0 (SuperSpeed) using a Cypress FX3. There are just a few requirements to the hardware design to use BeastLink.

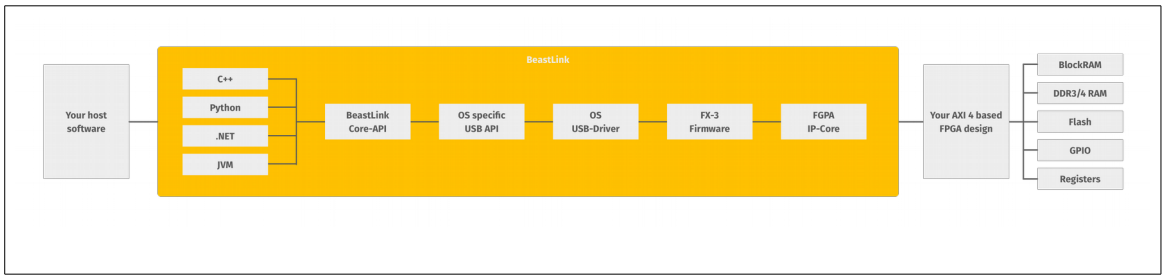
☑ Free Edition

☑ Pro Edition

Introduction

BeastLink is a set of components to allow transfer between the peripherals connected to an AXI-4 bus inside a Xilinx 7 Series FPGA and a PC over USB. Users don't have to understand any mechanism between the IP Core and the API on the host side. This is completely handled by BeastLink. It is very straightforward to adapt BeastLink to a new hardware, there are just few requirements to fulfill, primary a specific wiring between the Xilinx 7 Series FPGA and the Cypress FX3.

Following a schematic overview of BeastLink.



Overview

The Cypress FX3 is the core transfer element. It is able to communicate with the host without intervention by the FPGA. After connecting the FX3 to the host, the device is enumerated from host side using the vendor and product ID (VID/PID), that is stored in the flash connected to the FX3. If no ID is programmed (newly manufactured device), the Cypress FX3 uses a default VID/PID.

BeastLink contains a service (on Windows) and a UDEV rule (on Linux) that looks at newly connected USB-devices. If the device is known by the service (using a configuration file) the Cypress FX3 firmware gets downloaded to the FX3. After this is completed, the FX3 reconnects to the host, this time using the same VID, but with a different PID. This PID is the value stored in flash, but masked with 0x0800. The reason behind this is to prevent repeating the previous process, it is just unknown to the service, so a new firmware download is started. In addition to this re-enumeration, the firmware requests 900mA from the host (this is a feature of USB 3.0). After the host grants the usage, the Cypress FX3 enables the power to the FPGA.

After power-on, the FPGA tries to boot from its flash. If this is not possible, nothing happens. The host has the ability to **load** or **override** the active FPGA design at any time using a specific API command or with BeastLink Board Manager. This design must contain the BeastLink IP Core, so communication between host and AXI-4 bus is possible. From now on, the host can access the AXI-4 peripheral using specific API commands.

Each AXI-4 peripherals is mapped to a specific address range. The host API allows reading from and writing to all addresses inside the 32 bit address range. So if for example block RAM is mapped to address starting at 0x00000000, a write operation to address 0x00000010 will download data from host memory to the block RAM, starting at offset 0x00000010. A little specific transfer is register read and write. It essentially is just a 4 byte transfer to or from an address, but is usually used to configure or control a peripheral. Examples are:

- Access a range of 32 IO's
- Get status bits of a peripheral
- Read fill level of a FIFO
- Reset a peripheral

Components

Xilinx 7 Series FPGA IP Core

The IP Core is the bridge between the AXI-4 bus and the Cypress FX3. It manages all transfers between Cypress FX3 and FPGA and encodes and decodes the protocol that sits on top of the raw USB datastreams.

Cypress FX3 Firmware

The firmware is used to add features to the Cypress FX3, especially handling of the FPGA (power control, configuration, reset) and control of data transfer between USB and FPGA.

Host-PC driver parts & service

The driver is responsible to allow user space host software to access the USB bus. The service is used to download firmware to the FX3 upon connection.

Host-PC API

The API is separated into 2 parts. The core API wraps the OS specific USB API into a unique model (device enumeration, RAW transfer), handles specific requests to the FX3 and encodes and decodes the protocol on top of the raw USB datastreams (the opposite to the IP Core). The second layer maps the flat core API interface into an object-oriented manner to different programming languages and frameworks, specifically C++, Python and all .NET and JVM languages. For each supported language a well documented example application is available, showing:

- Device enumeration
- Gather device information
- Program the FPGA using the EFM-03 example design
- Write data into the block RAM and read it back

Host-PC Tools

There are 2 tools available. First one is BeastLink Board Manager, which allows

- Gathering device information
- Programming the FPGA using a design file
- Flashing an FPGA design and erase the flash subsequently
- Convert FPGA .bin files into source code, so the design can easily be compiled into an

application

The second tool is BeastLink Performance Monitor. This tool is useful to measure transfer speed between host and specific address ranges on the AXI-4 bus, e.g. block RAM. It has many options for testing and can be used to verify data integrity as well (write - read - verify).

Host-PC PTK

The PTK, aka Production Tool Kit is part of the Pro Edition and is a minimal application to test user build hardware, as well as prepare the FX3 flash using user specific VID and PID, as well as a serial number.

Revision history

Version	Date	Comment	Author	Approved
1.0	Feb, 26 2018	Initial release	th	mr

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CRITICAL APPLICATIONS

Address

CESYS Gesellschaft für angewandte Mikroelektronik mbH
Gustav-Hertz-Str. 4
D - 91074 Herzogenaurach
Germany